Through Silicon Via Technology:
The Ultimate Market for 3D Interconnect

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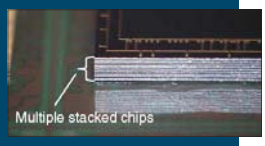

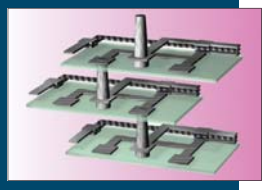

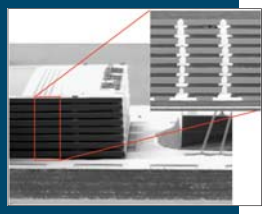

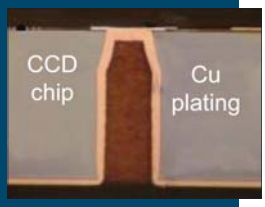

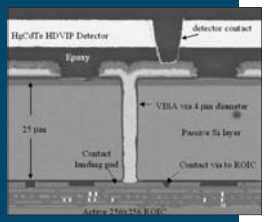

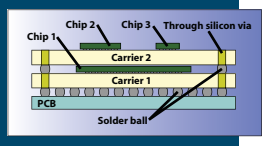

Through-hole silicon via (TSV) is the ultimate 3D interconnect. The industry is moving past the feasibility (R&D) phase for TSV technology into the commercialization phase where economic realities will determine which technologies are adopted. Low-cost fine via hole formation and highly reliable via filling technologies have been demonstrated; process equipment and materials are available. Even though design, thermal, and test issues remain, much progress has been made. Is 3D interconnect with TSV the answer to the interconnect crisis? Which technologies will be adopted? Will vias be formed during the wafer fabrication process or during IC packaging and assembly? What are the limitation factors to the adoption of this new technology? This report provides answers to these questions.

This TechSearch International report highlights the major processes and materials used by each company, including via fabrication methods, via filling, wafer thinning, and bonding methods. The report provides an update on activities of research organizations and key technologies used. A carefully developed forecast for market size in number of wafers is provided for each application area. Applications for 3D TSV include image sensors, flash, DRAM, processors, FPGAs, and power amplifiers. The timing for mass production depends on how the TSV compares in terms of cost with existing technologies. A timeline for the adoption of these applications is provided. Full text analysis provides critical details of the new developments and applications with photos and graphs of market projections.

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4 Research Organizations and Universities
ASET, CEA-LETI, EMC-3D Consortium, e-Cubes Project, Fraunhofer IZM Munich, IME, IMEC, ITRI, Lincoln Labs, MIT, Rensselaer Polytechinc Institute, Research Triangle Institute, Sematech, Tohoku University, University of Arkansas

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